

# SEMICONDUCTOR DEVICE, MANUFACTURING METHOD AND MOUNTING METHOD OF THE SEMICONDUCTOR DEVICE, CIRCUIT BOARD, AND ELECTRONIC APPARATUS

## BACKGROUND OF THE INVENTION

### 1. Field of Invention

[0001] The present invention relates to a semiconductor device, a manufacturing method and a mounting method of the semiconductor device, a circuit board, and an electronic apparatus.

### 2. Description of Related Art

[0002] Wafer level chip size package (CSP) is widely spreading as a package of a semiconductor device. In the related art, an orientation of a semiconductor device, as an end product, is specified by markings provided on the reverse of the element forming side on which its elements are formed. In other words, in related art, it is impossible to determine an orientation of a semiconductor device from the element forming side because of structural limitations of a semiconductor device. In particular, if a plurality of external terminals are disposed symmetrically, it is extremely difficult to determine an orientation of the semiconductor device according to its structure.

[0003] In the present invention an orientation of a semiconductor can be easily determined.

## SUMMARY OF THE INVENTION

[0004] (1) A semiconductor device according to one aspect of the present invention includes: a substrate having an electrode electrically connected to at least one integrated circuit; an external terminal electrically connected to the electrode; a light transmissive insulation layer disposed on the external terminal side of the substrate; and a mark provided on the substrate and covered by the insulation layer so as to be recognized through the insulation layer. According to an aspect of the present invention, an orientation of the semiconductor device can be easily determined by recognizing the mark through the insulation layer from the external terminal side of the substrate. Thus, an orientation of the semiconductor device can be determined from the structure of the semiconductor device in itself, enhancing handling efficiency of the semiconductor device.

[0005] (2) In this semiconductor device, the substrate can be a semiconductor substrate, and the integrated circuit can be formed on the semiconductor substrate.

[0006] (3) In the above semiconductor device, there are provided: a resin layer formed around the electrode and on the same side of the semiconductor substrate as the side provided with the electrode; and a interconnection layer extending from the electrode to the upper surface of the resin layer and including at least one land formed on the resin layer; the external terminal may be provided on the land; and the insulation layer may be formed to cover the interconnection layer with at least a part of the external terminal exposed.

[0007] (4) In the above semiconductor device, the mark may be provided on the resin layer.

[0008] (5) In the above semiconductor device, there is provided a passivation film provided on the semiconductor substrate, and the mark may be provided on the passivation film.

[0009] (6) In the above semiconductor device, the mark may be made of the same material as at least a part of the material which the interconnection layer is made of. Thus, for example, the interconnection layer and the mark are formed in the same manufacturing process.

[0010] (7) In the above semiconductor device, the mark may be provided on an area not contacting with the interconnection layer.

[0011] (8) In the above semiconductor device, the interconnection layer may include a plurality of lands including a first land having a shape incorporating the mark and a second land having a shape different from the shape of the first land. According to this, since a part or the whole of the first land serves as the mark, the number of components can be reduced.

[0012] (9) In the above semiconductor device, the external terminal may be a solder ball, and the insulation layer may be a solder resist.

[0013] (10) In the above semiconductor device, the semiconductor substrate may be a semiconductor chip.

[0014] (11) In the above semiconductor device, the mark may be provided on at least one of the four corners of the semiconductor chip.

[0015] (12) In the above semiconductor device, the semiconductor substrate may be a semiconductor wafer including the integrated circuit for each of plural areas.

[0016] (13) A circuit board according to another aspect of the present invention has a semiconductor device mentioned above mounted thereon.

[0017] (14) An electronic apparatus according to still another aspect of the present invention includes a semiconductor device mentioned above.

[0018] (15) A method of mounting a semiconductor device onto a circuit board according to still another aspect of the present invention includes: determining a mounting orientation of the semiconductor device mentioned above by recognizing the mark through the insulation layer.

[0019] (16) A method of manufacturing a semiconductor device according to still another aspect of the present invention includes: providing a mark on one side of a substrate having an electrode electrically connected to an integrated circuit; providing an external terminal electrically connected to the electrode on the mark side of the substrate; and providing a light transmissive insulation layer to cover the mark.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0020] FIG. 1 shows a plan view of a semiconductor device according to an exemplary embodiment of the present invention;

[0021] FIG. 2 shows a cross-sectional view of the semiconductor device according to an exemplary embodiment of the present invention;

[0022] FIG. 3 shows a partial plan view of a semiconductor device according to an exemplary embodiment of the present invention;

[0023] FIG. 4 shows a partial plan view of a semiconductor device according to an exemplary embodiment of the present invention;

[0024] FIG. 5 shows a partial plan view of a semiconductor device according to an exemplary embodiment of the present invention;

[0025] FIG. 6 shows a partial plan view of a semiconductor device according to an exemplary embodiment of the present invention;

[0026] FIG. 7 shows a partial plan view of a semiconductor device according to an exemplary embodiment of the present invention;

[0027] FIG. 8 shows a partial plan view of a semiconductor device according to an exemplary embodiment of the present invention;

[0028] FIG. 9 shows a circuit board according to an exemplary embodiment of the present invention;

[0029] FIG. 10 shows an electronic apparatus according to an exemplary embodiment of the present invention; and

[0030] FIG. 11 shows an electronic apparatus according to an exemplary embodiment of the present invention.

#### DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0031] Hereinafter, exemplary embodiments of the present invention are explained referring to accompanying figures.

[0032] FIG. 1 shows a plan view of a semiconductor device of the present exemplary embodiment with a part (a insulation layer 50) thereof removed. FIG. 2 shows a cross-sectional view (a section along II-II plane in FIG. 1) of the semiconductor device of the present exemplary embodiment. FIGS. 3 through 6 show partial plan views of semiconductor devices showing other examples of the mark.

[0033] A semiconductor device 1 includes a substrate (a semiconductor substrate 10 in the present exemplary embodiment). The semiconductor substrate 10 can be a semiconductor chip as shown in FIG. 1 or a semiconductor wafer. The semiconductor substrate 10 is provided with an integrated circuit 12 formed thereon (See FIG. 2.) and further with an electrode (e.g., a pad) 14 electrically connected with the integrated circuit 12. In case of a semiconductor ship, the integrated circuit 12 is often formed on a single region, while the integrated circuit 12 is often formed on each of multiple regions in case of a semiconductor wafer. A plurality of electrodes 14 may be formed on either surface of the semiconductor substrate 10. The plurality of electrodes 14 can be arranged along an edge portion (e.g., two opposing sides or four sides) of the semiconductor chip (or a region to become the semiconductor chip). The side of the semiconductor substrate 10 (the side with the electrode 14 formed thereon) is provided with a passivation film (e.g., a silicon nitride film or a silicon oxide film) 16 formed thereon.

[0034] In the present exemplary embodiment, the side of the semiconductor substrate 10 (e.g., a surface of the passivation film 16) provided with the electrode 14 is further provided with a resin layer 18 including a single layer or multiple layers. The resin layer 18 is formed around the electrodes 14. As shown in FIG. 1, the resin layer 18 can be formed on a center portion of the semiconductor chip. The resin layer 18 may have a side face slanted so that the bottom surface thereof is larger than the opposing upper surface thereof. The resin layer 18 may have a tension reduction function. The resin layer 18 may be made of resin, such as polyimide resin, silicone-modified polyimide resin, epoxy resin, silicone-modified epoxy resin, benzocyclobutene (BCB), or polybenzoxazole (PBO). The

resin layer 18 may be formed between the semiconductor substrate 10 and an external terminal 40 described later.

**[0035]** In the present exemplary embodiment, the semiconductor device 1 includes interconnection layer 20. The interconnection layer 20 is formed on the same side of the semiconductor substrate 10 as the side provided with the electrode 14. The interconnection layer 20 is made of conductive material (e.g., metal). A plurality of discrete regions of the interconnection layer 20 is formed as shown in FIG. 1 each consisting of one or more layers. In case of plural layers, the interconnection layer 20 may be made of a combination of a plurality of different materials (e.g., copper (Cu), chromium (Cr), titanium (Ti), nickel (Ni), titanium-tungsten (TiW), gold (Au), aluminum (Al), nickel-vanadium (NiV), tungsten (W), etc.). The discrete regions of the interconnection layer 20 are formed to cover the electrodes 14 and electrically connected with the electrodes 14. The discrete regions of the interconnection layer 20 extend from the electrodes 14 onto the resin layer 18. The discrete regions of the interconnection layer 20 are formed so as to extend to the upper surface of the resin layer 18 through its side face (the slanted face).

**[0036]** The discrete regions of the interconnection layer 20 include plural lands (a first and second lands 22, 24 in the present exemplary embodiment). The lands are electrical terminals, and provided with plated layers (not shown in the figures) to enhance electrical characteristics. The lands are formed on the resin layer 18. The lands are wider than lines of the discrete regions of the interconnection layer 20, and can be shaped as, for example round lands.

**[0037]** The semiconductor device 1 includes a plurality of external terminals 40. The external terminals 40 are formed on the same side of the semiconductor substrate 10 as the side on which the electrodes 14 are formed. The external terminals 40 are electrically connected to the electrodes 14. As shown in FIGS. 1 and 2, the external terminals 40 are electrically connected to the discrete regions of the interconnection layer 20. The external terminals 40 can be formed on the lands. The external terminals 40 can be made of conductive metal. The external terminals 40 can also be made of brazing material. The external terminals 40 can be shaped as, for example, a sphere, and can be solder balls. In the example shown in FIG. 1, the plurality of external terminals 40 is disposed symmetrically in plan view of the semiconductor substrate 10.

**[0038]** The semiconductor device 1 includes an insulation layer 50 (e.g., a layer made of resin). The insulation layer 50 has translucency, and can be made of translucent or

transparent material. The insulation layer 50 is formed of a single or multiple layers (a first and second insulation layers 54, 52 in the example shown in FIG. 2). The insulation layer 50 is formed on the same side of the semiconductor substrate 10 as the side on which the external terminals 40 are formed. In detail, the insulation layer 50 is formed to cover the interconnection layer 20 with at least a part of the external terminals 40 exposed (with the tip of the external terminals 40 exposed). The insulation layer 50 can also serve as a solder resist.

**[0039]** In the example shown in FIG. 2, the insulation layer 50 includes the first and the second insulation layers 54, 52. The first and the second insulation layers 54, 52 are translucent as described above. The first insulation layer 54 can be formed after fabrication of the interconnection layer 20 so as to cover at least a part of each of the discrete regions of the interconnection layer 20. As shown in FIG. 2, the first insulation layer 54 can be formed outside at least center portions of the lands. Oxidization, corrosion, or breaking of the interconnection layer 20 can be avoided by forming the first insulation layer 54.

**[0040]** The second insulation layer 52 is stacked on the first insulation layer 54. The second insulation layer 52 can be formed on the first insulation layer 54 after fabrication of the external terminals 40. The second insulation layer 52 is formed with tip portions of the external terminals 40 exposed. In this case, the second insulation layer 52 covers root portions (lower end portions) of the external terminals 40. Thus, the root portions of the external terminals 40 are reinforced.

**[0041]** The semiconductor device 1 includes a mark 30. The mark 30 is formed on the same side of the semiconductor substrate 10 as the side on which the external terminals 40 are formed (e.g., on the resin layer 18), and is covered with the insulation layer 50 (the first and the second insulation layers 54, 52 in FIG. 2). Since the insulation layer 50 has translucency, the mark 30 can be recognized through the insulation layer 50. Thus, since the insulation layer 50 is provided on the mark 30, breakage, separation, or discoloration caused by oxidization can be reduced or prevented ensuring that an orientation of a semiconductor device is determined using the mark 30.

**[0042]** The position or the shape of the mark 30 is arranged so that at least an orientation (plan orientation) of the semiconductor device 1 (or the semiconductor substrate 10) can be acknowledged. For example, the mark 30 may be formed to have a shape by which either direction can be recognized (e.g., a shape of an arrow or the like). Or, the mark 30 may be disposed at an end portion of the semiconductor substrate 10 (e.g., at a corner

thereof). Thus, an orientation of the semiconductor device can be determined only by recognizing the position of the mark 30 (even if its shape cannot be recognized). Note that the mark 30 may be a single mark or a plurality of marks as well.

**[0043]** The mark 30 can be made of the same material as at least a part of the interconnection layer 20 (at least one layer if the interconnection layer 20 comprises multiple layers). For example, if the interconnection layer 20 is made of metal, the mark 30 may also be made of the metal. If the interconnection layer 20 includes multiple layers, the mark 30 may also include the multiple layers. By this structure, the mark 30 may be formed in the process for forming the interconnection layer 20, thus reducing the cost and the number of manufacturing processes.

**[0044]** In the example shown in FIGS. 1 and 2, any one of the plural lands has the mark 30 as its part. In further detail, the shape of the first land 22, provided at least one includes the mark 30, and the shape of the second land 24, is different from the shape of the first land 22. In the example shown in FIG. 1, the shape of the first land 22 includes a round part and a protrusion (a quadrangular part in FIG. 1) protruding from the round part, one of the external terminals 40 being provided on a center portion of the round part, and the protrusion serving as the mark 30. The protrusion may be provided on the opposite side of the first land 22 to the line thereof. For example, the first land 22 as a whole may be recognized as the mark 30. According to this, since the part or the whole of the first land 22 serves as the mark 30, the number of components of the semiconductor device can be reduced. Further, space of the semiconductor device can be efficiently used compared to the case of forming the mark 30 independently. This is especially efficient for application to CSP (chip size package) in which the sizes of the semiconductor device and the semiconductor chip are substantially the same.

**[0045]** The shape of the mark (or the surface shape of the first land 22) is not limited, but may be modified to various shapes as shown in FIGS. 3 through 6. As shown in FIG. 3, the protrusion as a mark 32 may be shaped as a triangle. As shown in FIG. 4, the protrusion as a mark 34 may be shaped as a combination of multiple polygons (e.g., a convex shape). As shown in FIG. 5, the position of the protrusion as a mark 36 may not be limited to the opposite side to a line of the first land 22, but the protrusion can be, for example, positioned at the point having a normal perpendicular to a normal at the line. As shown in FIG. 6, the plural protrusions as marks 38 may be disposed at plural positions (e.g., the both positions shown in FIGS. 1 and 5).

**[0046]** As a modification of the present exemplary embodiment, a mark 60 (a mark 62) may be provided independently from discrete regions of the interconnection layer 20, as shown in FIGS. 7 and 8. That is, the mark 60 (the mark 62) may be provided on a region not contacting the discrete regions of the interconnection layer 20 (the land 22). As an example shown in FIG. 7, the mark 60 can be formed on a passivation 16 (See FIG. 2.) in the same process as that for the interconnection layer 20, as previously described. As an example shown in FIG. 8, the mark 62 may be formed on the resin layer 18 in the same process as that for the interconnection layer 20, as previously described. According to the above, since the mark may be provided without any limitations derived from the position of the land, the mark may be provided on a position easy to be recognized resulting in easy determination of an orientation of the semiconductor device. Furthermore, since the mark need not be positioned adjacent to the discrete regions of the interconnection layer 20, the flexibility of the interconnection layer 20 in wiring from electrodes 14 to the land 22 can be enhanced. Also, as shown in FIGS. 7 and 8, the mark 60 (the mark 62) may be provided at least one of the four corners of the semiconductor chip.

**[0047]** As a modification of the present exemplary embodiment, the semiconductor device may include a substrate (e.g., an interposer) and a semiconductor chip (on which an integrated circuit is formed) mounted on the substrate. In this case, there is formed on the substrate an electrode (e.g., a terminal portion of an interconnection pattern) electrically connected to the integrated circuit of the semiconductor chip. A mark to determine an orientation of the semiconductor device is formed on the substrate (more precisely, on the same side of the substrate as the side provided with the electrode).

**[0048]** According to the semiconductor device of the present exemplary embodiment, by recognizing the mark 30 through the insulation layer 50 from the external terminals 40 side of the substrate (the semiconductor substrate 10), an orientation of the semiconductor device can easily be determined. Thus, an orientation of the semiconductor device can be determined from the structure of the semiconductor device in itself offering high efficiency in handling of the semiconductor device.

**[0049]** A semiconductor device manufacturing method according to another exemplary embodiment includes: forming the mark 30 on one side (e.g., the side on which the electrodes 14 are formed) of the substrate (the semiconductor substrate 10 in the present exemplary embodiment); forming the external terminals 40 on the same side of the semiconductor device as the side provided with the mark 30; and providing the insulation



layer 50 so as to cover the mark 30. Since the insulation layer 50 has translucency as previously described, the mark 30 can be recognized through the insulation layer 50. If the semiconductor wafer is used as the semiconductor substrate 10, the semiconductor substrate 10 is cut into plural regions each corresponding to the integrated circuit 12. A plurality of semiconductor devices is obtained by cutting the semiconductor substrate 10. In this case, packaging is performed every wafer. Note that other details and advantages of the present exemplary embodiment can be reached from the above description regarding the semiconductor device, and therefore are omitted from the description of this section.

**[0050]** A semiconductor device mounting method according to still another exemplary embodiment includes mounting the semiconductor device 1 (including a semiconductor chip) on a circuit board (e.g., a mother-board (See FIG. 9.)), and a mounting orientation of the semiconductor device 1 is determined by recognizing the mark 30 through the insulation layer 50. According to the above, the orientation of the semiconductor device can be determined from the structure thereof in itself. Note that other details and advantages of the present exemplary embodiment can be reached from the above description regarding the semiconductor device, and therefore are omitted from the description of this section.

**[0051]** FIG. 9 shows a circuit board 1000 according to still another exemplary embodiment of the present invention having the semiconductor device 1 mounted thereon. As an electronic apparatus according to still another exemplary embodiment of the present invention including the semiconductor device, FIG. 10 shows a laptop personal computer 2000, and FIG. 11 shows a cellular phone 3000.

**[0052]** The present invention is not limited to the aforementioned exemplary embodiments, but various modifications thereof are possible. For example, the present invention may include substantially the same structures as explained in the description of the exemplary embodiments (e.g., structures with the same function, way, and results or structures with the same objects and results). Furthermore, the present invention may include structures obtained by replacing a nonessential part of the structure explained in the description of the exemplary embodiments. Still further, the present invention may include structures offering the same action and results or structures achieving the same object as the structures explained in the description of the exemplary embodiments. Still further, the present invention includes structures obtained by combining prior art with the structure explained in the description of the exemplary embodiments.